University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences
Spring 2025EE 130/230A Integrated Circuit (IC) Devices

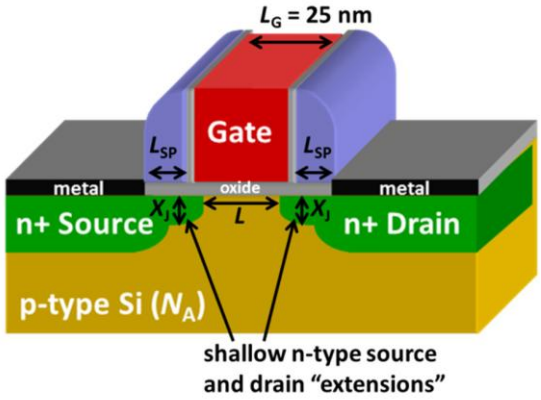
NMOSFET Design Project

You may complete the project either individually or in groups of two people.

In this project, you will use semiconductor device simulation software (Synopsys' Sentaurus package) to design an **N-channel Si MOSFET** with gate length, L_G **= 25 nm** (relevant for the "20 nm generation" of CMOS technology) to meet specified performance requirements within some practical design constraints. The simulator represents the transistor structure as a mesh of points, keeping track of the material properties and net dopant concentration (within a semiconductor material) at each point and self-consistently solving the Poisson equation and continuity equations to find the mobile charge carrier (electron and hole) concentrations, electric field, electric potential, and current flow at each point. Analytical models are used to calculate the effective mass and carrier mobilities and to account for phenomena such as band gap narrowing, generation-recombination, band-to-band (Zener) tunneling, and velocity saturation. For a specified transistor structure and operating conditions (*e.g.*, bias voltages and temperature), terminal currents can be derived. If the transistor structure were described in two dimensions (as is the case for this project), then, the simulator would assume that the transistor width (*i.e.*, the MOSFET channel width) is **1 µm**.

MOSFET Structure

The channel region and "body" of the MOSFET are **uniformly-doped P-type**, with dopant concentration N_A. To mitigate the short-channel effect, the MOSFET structure comprises **shallow N-type source/drain "extension"** regions adjacent to the channel region; to mitigate parasitic series resistance, **deeper and more heavily doped junctions** are used in the regions where metallic contacts are made to the source and drain.



In practice, the N-type source/drain extension (SDE) regions are formed by implantation of dopants into the Si; the gate electrode blocks this implant from reaching the channel region, so that the SDE regions are naturally aligned to the gate electrode edges. The **SDE junction depth** X_J is determined by the implantation energy and post-implant thermal annealing conditions. (Annealing at a high temperature—typically greater than 900 ˚C—is necessary to repair the implantation induced damage to the crystalline lattice, such that dopant atoms reside on Si lattice sites.) Due to lateral "straggle" inherent to the implantation process, and dopant diffusion during the high-temperature annealing step, the channel length L is slightly smaller than the gate length L_G; **the deeper** X_J **is, the smaller** L **is**. The deep N^+ source/drain regions are also formed by implantation of dopants (but at a higher energy and dosage than used to form the SDE regions), after the formation of dielectric (SiO_2 and/or Si_3N_4) **"spacers" of length** L_{SP} along the sidewalls of the gate electrode. The spacers serve to block this implant so that the deep source/drain regions are offset from the channel region. The longer L_{SP} is, the longer the length of the SDE regions (which have higher resistivity than the deep source/drain regions).

Fixed Design Parameters

Values for the following transistor parameters are **fixed** (i.e., you will not be allowed to adjust them), based on the *International Technology Roadmap for Semiconductors, 2011 Ed.* (Process Integration, Devices, and Structures Chapter), which is available online at https://www.semiconductors.org/wp-content/uploads/2018/08/2011PIDS.pdf

- Gate length: $\boldsymbol{L_G}$ **= 25 nm**
- Effective oxide thickness: $\boldsymbol{T_{oxe}}$ **= 1 nm**
- Gate work function = **4.6 eV** (corresponding to Titanium Nitride)
- Deep source/drain regions:
  - o Dopant concentration vs. depth profile is **Gaussian**
  - o Peak dopant concentration = $\mathbf{2\times10^{20}\ cm^{-3}}$
  - o Junction depth (defined as the distance from the Si surface to the depth, where the deep source/drain dopant concentration is equal to the body dopant concentration) = **25 nm**
- Source/drain extension regions:
  - o Dopant concentration vs. depth profile is **Gaussian**
  - o Peak dopant concentration = $\mathbf{9\times10^{19}\ cm^{-3}}$

The power supply voltage, $\mathbf{V_{DD} = 0.8V}$. The body bias voltage, $\mathbf{V_B = 0\ V}$.

Design Task

Co-optimize the channel/body dopant concentration N_A, SDE junction depth X_J, and spacer length L_{SP}, in order to meet the following MOSFET performance specifications:

- $\boldsymbol{I_{OFF} \leq 1}$ **nA per µm channel width,**
- $\boldsymbol{I_{ON} \geq 400}$ **µA per µm channel width,**

with the following practical design constraints:

- $1\times10^{17}\ cm^{-3} \leq N_A \leq 4\times10^{18}\ cm^{-3}$,
- $10\ nm \leq L_{SP} \leq 35\ nm$,
- $4\ nm \leq X_J \leq 20\ nm$.

I_{ON} is defined to be I_{DS} for $V_{GS} = V_{DS} = V_{DD}$, and
I_{OFF} is defined to be I_{DS} for $V_{GS} = 0$ V and $V_{DS} = V_{DD}$. This will correspond to a **low operating power design**.

Larger I_{ON} provides for faster (or higher frequency) circuit operation, while lower I_{OFF} provides for lower static power consumption; therefore, a high I_{ON}/I_{OFF} ratio is generally desirable. You should explore the **trade-offs between $\boldsymbol{I_{ON}}$ and $\boldsymbol{I_{OFF}}$** by simulating the transfer characteristic (I_{DS} *vs.* V_{GS} curve) for different combinations of values for the three design parameters:

- Increasing N_A increases V_T and hence reduces I_{OFF} (unless N_A is so large that band-to-band tunneling at the drain junction becomes significant), but degrades the effective mobility and hence I_{ON}.
- Smaller X_J depth helps to reduce the short-channel effect and hence I_{OFF}, but results in larger parasitic series resistance and hence degrades I_{ON}.
- Longer spacers help to reduce the influence of the deep source/drain regions on the channel region but result in larger parasitic series resistance.

Rubric for Project Report

For your finalized MOSFET design:

1. [20 pts] Illustrate your MOSFET design, labeling and indicating your values for the design parameters. Describe the process (in a paragraph) by which you arrived at your final design.

2. [20 pts] Run the I_{DS}-V_{GS} simulation for V_{DS} = 50 mV (corresponding to the linear region of operation) and for $V_{DS} = V_{DD}$ (corresponding to the saturation region of operation) and plot the $\boldsymbol{I_{DS}}$-$\boldsymbol{V_{GS}}$ **curves for** $\boldsymbol{0 \le V_{GS} \le V_{DD}}$. Manually extract the following performance parameters from the simulation outputs:
   - **Minimum subthreshold swing** (S).
   - **Linear threshold voltage** (V_{Tlin}), defined as the value of V_{GS} corresponding to I_{DS} = 100 nA × W/L at V_{DS} = 50 mV. Note that the saturation threshold voltage (V_{Tsat}), defined as the value of V_{GS} corresponding to I_{DS} = 100 nA × W/L at $V_{DS} = V_{DD}$, is automatically extracted for you by the simulation package.
   - **Drain-induced barrier lowering** (DIBL), in units of mV per Volt, defined as
   $$\text{DIBL} = \frac{|V_{\text{Tlin}}| - |V_{\text{Tsat}}|}{V_{\text{DD}} - V_{\text{Dlin}}}$$

3. [10 pts] What is the **threshold voltage** (V_T) calculated using the MOSCAP theory as mentioned in the textbook? Briefly explain why it's different from the values obtained in Question 2 above.

4. [20 pts] Run I_{DS}-V_{DS} simulations for V_{GS} = 0.5, 0.6, 0.7, and 0.8 V and plot the $\boldsymbol{I_{DS}}$-$\boldsymbol{V_{DS}}$ **curves for** $\boldsymbol{0 \le V_{DS} \le V_{DD}}$**. Does your designed MOSFET exhibit a square-law dependence of saturation current on** $\boldsymbol{V_{GS}}$**?** Briefly explain.

5. [10 pts] Change the effective oxide thickness (EOT) to 3 nm and comment on how that changes the I_{DS}-V_{GS} at $V_{DS} = V_{DD}$. Please comment on how oxide thickness will affect the future generations when gate length is further reduced?

6. [10 pts] If we'd like to reduce OFF current significantly without giving up ON current too much, *i.e.*, increase the ON/OFF ratio while keeping the ON current almost intact, then, what design modifications would you suggest? Justify your answer. For this question, you are allowed to modify the parameters that were fixed earlier (listed under the heading 'Fixed Design Parameters'), except for the channel length, which still has to be 25 nm.

7. [10 pts] How would you expect the ON current, OFF current, and subthreshold swing to change with increasing temperature (*e.g.* to 85 degrees Celsius)? Briefly explain.

Submission Instructions

The deadline for the project is **5/9/2025 (Friday) 11:59pm PST.**
Please submit on bCourses the following:

1) the project report that meets the criteria above in .pdf file format
2) the completed Sentaurus program that you modified and optimized to satisfy the design task, in .zip file format

If you worked individually, please write your name on the first page of the report and submit your report on bCourses.
If you worked with a partner, both your names should be on the first page of the report, and only one person should submit the report and code on bCourses.