EE130 Final Project Report

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Q1: Summary of final chosen parameters and diagram

- $X_0 = 1 \times 10^{-3}$
- $L_{gate} = 0.025\ \mu m = 25\ nm$
- $L_{sp} = 0.015\ \mu m = 15\ nm$
- Channel doping $(N_A) = 1 \times 10^{18}\ cm^{-3}$
- $X_{jext} = 0.004\ \mu m = 4\ nm$
- $ID_{sat} / I_{on} = 4.154 \times 10^{-4} A/\mu m\ channel\ width$
- $I_{off} = 7.269 \times 10^{-10} A/\mu m\ channel\ width$

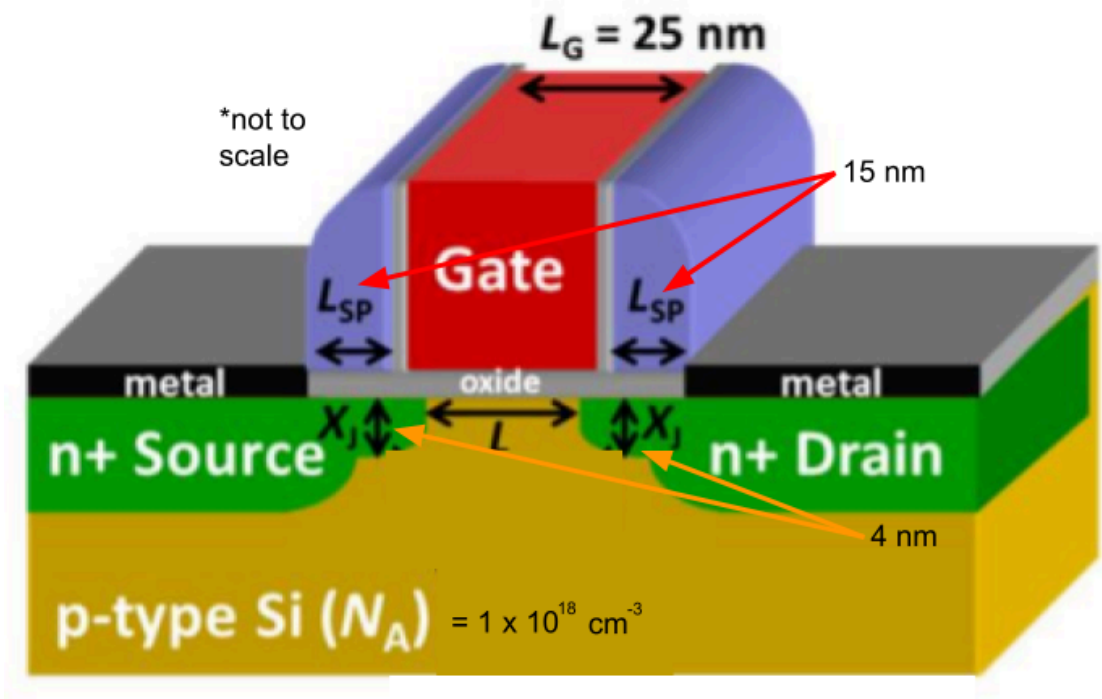

Figure 1: Diagram of compliant nMOSFET with chosen process parameters labeled

Q1: Process description

We first read and observed how increasing N_A reduces I_{off}, and increases I_{on}. Decreasing X_j increases I_{off} but decreases I_{on}. Increasing L_{sp} decreases I_{off} but does not significantly affect I_{on}. We confirmed all of these patterns by running preliminary analysis in Sentaurus, changing each independent variable one by

one in a positive and negative direction and observing the effects on the dependent variables, I_{on} and I_{off}. We decided to run a simulation iteratively on different values for L_{sp}, channel doping (N_A), and X_j. For L_{sp}, we had 6 different values: 0.010, 0.015, 0.020, 0.025, 0.030, 0.035. For chanel doping, we had 7 different values: $1.00e^{17}$, $8.8e^{17}$, $1.00e^{18}$, $1.66e^{18}$, $2.44e^{18}$, $3.22e^{18}$, $4.00e^{18}$. For X_j, we had 6 different values: 0.013, 0.004, 0.008, 0.012, 0.016, 0.02. These values were chosen based on the proposed ranges given in the project description; we manually determined the step size so as to generate a reasonable number of values, balancing granularity and run time. This process generated a total of 252 different simulations (row). 1 out of 252 simulation outputs values for I_{on} and I_{off} that meets the requirement, as specified in the previous section. Values:

- $I_{on} = 4.154 \times 10^{-4} A/\mu m\ channel\ width \geq 400\ \mu A/\mu m\ channel\ width$ ✓
- $I_{off} = 7.269 \times 10^{-10}\ A/\mu m\ channel\ width \leq 1\ nA/\mu m\ channel\ width$ ✓

Q2: I(DS) vs V(GS) and Performance Parameters

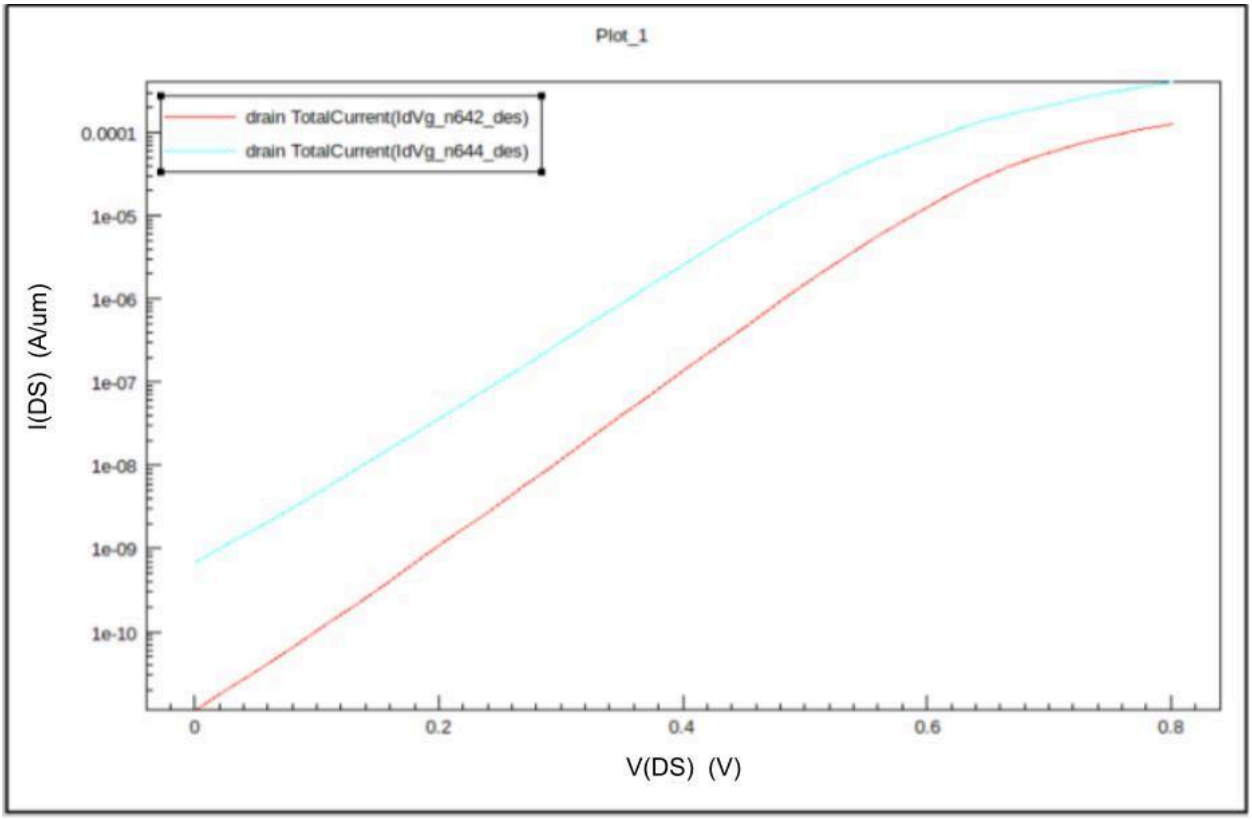

Figure 2: Graph of I_{DS} vs. V_{GS} plotted for $V_{D(lin)} = 0.05\ V$ (red) and $V_{D(lin)} = 0.8\ V$ (blue)

Min subthreshold swing can be calculated by calculating the *maximum* slope (since S = $1/slope$) of the linear region of the plot. By inspection, this would be the red / 0.05V line in this case. $V_{T(lin)}$ can be read

off the red graph as V_{DS} where $I_{DS} = 100\ nA/\mu m = 1x1-^{-7}\mu A/\mu m$. DIBL can be calculated by using the equation given in the report spec sheet.

Minimum Subthreshold Swing

$$S = \frac{dV_{GS}}{d(\log I_D)} = \frac{0.2915 - 0.1946}{\log(10^{-8}) - \log(10^{-9})} = 0.0969 = 96.9\ mV/Decade$$

$V_{T(lin)}$ = 0.540V

DIBL

$$DIBL = \frac{|V_{Tlin}| - |V_{Tsat}|}{V_{DD} - V_{Dlin}} = \frac{0.540 - 0.419}{0.8 - 0.05} = 0.1613 = 161.3\ mV/V$$

Q3: V(th) Calculation

$$\phi_F = kT \ln\left(\frac{N_A}{n_i}\right)$$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\epsilon_s|2\phi_F|}}{(\epsilon_{ox}/t_{ox})}$$

$$\phi_F = 0.026 \ln\left(\frac{10^{18}}{10^{10}}\right) = 0.4789$$

$$2\phi_F = 0.958$$

$$\frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{10^{-7}} = 0.00000003453$$

$$V_{FB} = \Phi_G - \Phi_s = \Phi_g - \left(\chi_s + \frac{E_g}{2} + \phi_F\right)$$

$$= 4.6 - (4.05 + 0.56 + 0.4789)$$

$$= -0.4889\ V$$

$$V_T = -0.4889 + 0.958 + \frac{\sqrt{2(1.6)(10^{-19})(10^{18})(11.8)(8.854)(10^{-14})(0.958)}}{0.00000003453}$$

$$= 0.633\ V$$

The calculated V_T is different from V_T in Q2 because of the non-ideality in this real life MOSFET. The MOSFET has a short channel length and effects like Drain-Induced Barrier Lowering (DIBL) can significantly reduce V_T as shown in question 2.

Q4: I(DS)-V(DS) Simulation

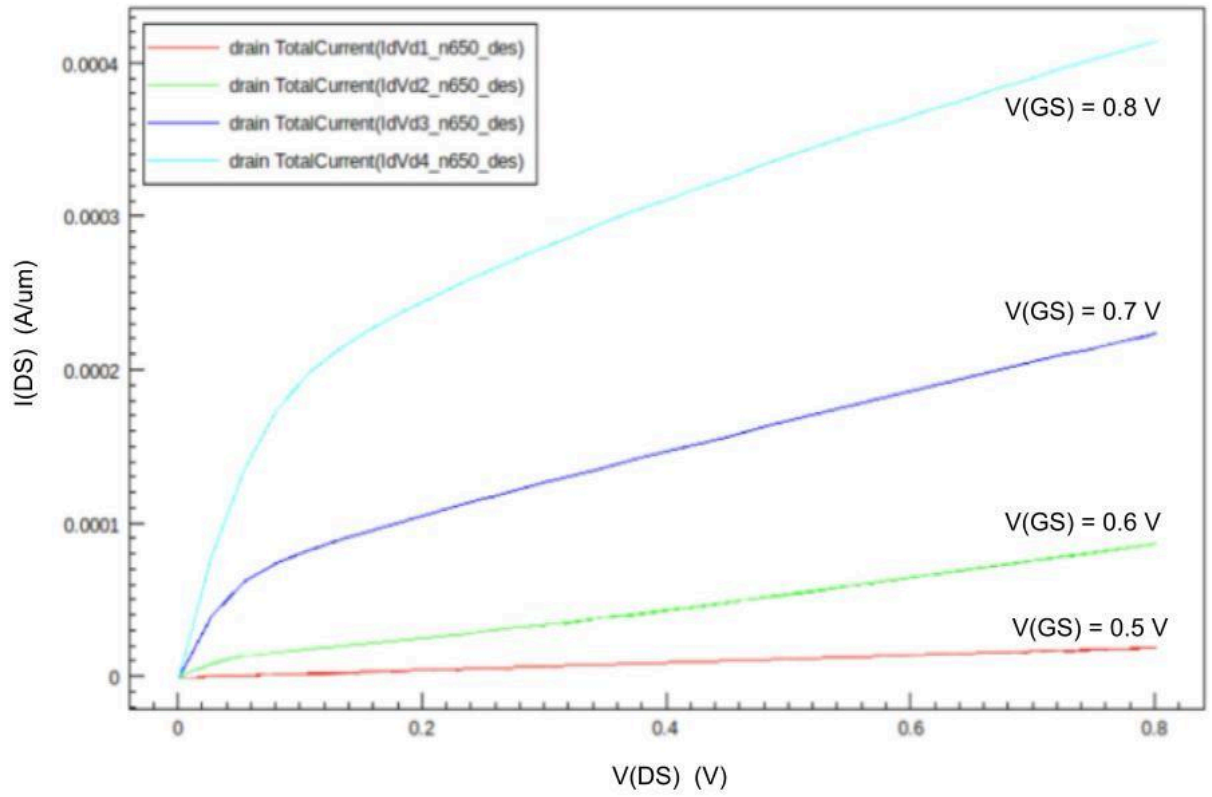

Figure 3: Graph of V_{DS} VS. I_{DS} for different V_{GS} values

In the graph above, V_{DS} is plotted on the x axis and I_{DS} plotted on the y axis. As V_{GS} is varied from 0.5 to 0.8 V in increments of 0.1 V, the graph exhibits characteristics of the square law dependence. Firstly, we observe 3 distinct regions of the graph, especially at higher V_{GS} values. These regions are from left to right: the linear region, the saturation knee (occurs at $V_{DS} = V_G - V_T$), and the saturation region (which is a flat plateau to the right). These regions are also marked on our plot for $V_{GS} = 0.8\,V$.

Linearity occurs because at lower V_{DS}, a continuous inversion sheet spans from source to drain and the MOSFET behaves like a gate-voltage-controlled resistor. Saturation knee occurs when the channel just pinches off at the drain end. At the saturation region, we should normally have a flat plateau in current because increasing V_{DS} past a certain point merely widens the depletion wedge and no extra charge can be supplied. However, in our case, we must apply the short channel assumption ($L << L_{dep}$) as we observe the current continuing to increase linearly past the saturation knees. This occurs when the channel width is small and increases the tangential electric field, causing carrier velocity to saturate. Under this regime, $I_{D(sat)}$ becomes proportional to $V_G - V_T$ instead of $(V_G - V_T)^2$, giving the shape seen above.

Q5: Changing EOT

The following effects occur when we increase the effective oxide threshold:

- Increasing t_{ox} decreases C_{ox} which increase V_T, by the formula given in Q2
- Subthreshold swing, specifically the η term, would increase since C_{ox} decreases
- I_{sat} decreases since: V_T increases and C_{ox} decreases

For our graph, this means that the slope of linear region is lower (device turns on more gradually), the "elbow" shifts right due to increased V_T, and I_{sat} is lowered. Essentially, our curve shifts down and right.

As gate length is reduced further for future generations of MOSFETs to create smaller devices, thick EOT is detrimental to overall performance. Thick EOTs move subthreshold swing away from the optimal 60 mV/dec theoretical limit and also increase DIBL for small gate lengths. Thick EOTs also increase threshold voltage, and most detrimentally, increase I_{on}. All of these factors make the switching nature of the MOSFET more unpredictable to work with and/or increase power consumption. At the same time, reducing EOT too much (beyond 1 nm) will create quantum tunneling effects and large leakage currents. The ideal EOT is thus at a "happy medium" between too thick and too thin. In summary, EOT is a crucial rate limiting factor for the development of future MOSFETs and is a parameter that must be thought about critically during design.

Q6: On/Off Current Optimization

In order to optimize the on/off current we re-examined our variable choices and the trends observed in Question 1. We decided to focus on L_{sp} since we observed that increasing L_{sp} reduced I_{off} and had a relatively small impact on I_{on}. We quantified this relationship further by changing L_{sp} and observing the impacts on I_{on} and I_{off}.

L_{sp}	I_{on}	I_{off}
0.01	$6.223x10^{-4}$	$9.904x10^{-10}$
0.015	$4.154x10^{-4}$	$7.269x10^{-10}$
0.02	$3.090x10^{-4}$	$6.032x10^{-11}$
0.025	$2.493x10^{-4}$	$1.588x10^{-11}$
0.03	$2.111x10^{-4}$	$7.753x10^{-12}$
0.035	$1.853x10^{-4}$	$5.216x10^{-12}$

Table 1: Table showing the effects of changing L_{sp}, where yellow row highlights the values of I_{on} and I_{off} using the L_{sp} defined in Q1

As seen in the data, as L_{sp} is increased from 0.015 μm to 0.035 μm, the off current drops by two orders of magnitude. At the same time, the on current decreases by less than an order of magnitude. While this still represents a decrease, this is relatively low compared to the much larger leakage suppression.

The explanation for this is that high DIBL decreases V_t, as seen in question 2 and 3. A longer L_{sp} increases the physical distance between the drain and the channel (reduces leakage). Increasing L_{sp} reduces DIBL without having to change the gate length. Therefore, reducing DIBL increases V_t, which would also decrease I_{off} by the square law. I_{on} would not change significantly because the $(V_G - V_t)$ term in the square law equation is only slightly reduced since V_t is not changing drastically.

Thus, increasing L_{sp} is an effective strategy for improving the on/off current ratio: it significantly reduces off current while maintaining acceptable on state performance.

Q7: Effects of Increasing Temperature

- I_{on} decreases. Carrier mobility decreases due to stronger phonon scattering at higher temperatures, i.e. phonons bump into electrons more often, causing electrons to drift more slowly. Note that threshold voltage is also lowered due to barrier height being lowered (more molecules in high energy states at higher temperatures) but the drop in carrier mobility is "stronger" mathematically.
- I_{off} increases. As mentioned above, the lower barrier height means more electrons can go over / tunnel through the barrier. Additionally, higher temperatures boost intrinsic carrier generation in the bulk silicon due to increased vibrations. All of these factors increase carrier leakage.
- Subthreshold swing increases. Because there are more carriers closer to the conduction band, changing surface potential at high temperature adds fewer new carriers than the same process at room temperature. Therefore, a larger gate voltage change is required to achieve the same decade change in drain current. By definition, this increases S.